**IN THE CLAIMS:**

1. (Previously Presented) A method of fabricating a semiconductor device, comprising:

(a) forming an oxide film entirely over a semiconductor substrate on which a MOS transistor is fabricated;

(b) carrying out spike rapid thermal annealing (RTA) as first therma-annealing to said semiconductor substrate;

(c) selectively removing said oxide film in an area where later mentioned semiconductor-metal compound is to be formed while leaving oxide film in a non-silicide transistor region;

(d) forming a metal film entirely over said semiconductor substrate; and

carrying out second thermal-annealing to said semiconductor substrate to form semiconductor-metal compound in said area.

2. (Previously Presented) The method as set forth in claim 1, further comprising (f) removing said metal film having been not reacted with said semiconductor substrate.

3. (Previously Presented) The method as set forth in claim 1, wherein said semiconductor substrate is a silicon substrate, and said semiconductor-metal compound is silicide.

4. (Previously Presented) The method as set forth in claim 3, wherein said metal film is composed of cobalt, tungsten or titanium.

5. (Previously Presented) The method as set forth in claim 1, wherein said oxide film is formed by chemical vapor deposition (CVD) in the range of 300 to 500 degrees centigrade both inclusive by the thickness of 20 to 40 nanometers both inclusive.

6. (Previously Presented) The method as set forth in claim1, wherein said spike rapid thermal annealing (RTA) is carried out by zero second in the range of 1000 to 1100 degrees centigrade.

7. (Previously Presented) The method as set forth in claim 1, wherein said first thermal-annealing is carried out also for activating impurities having been implanted into source and drain regions of said MOS transistor, and for removing defects in said source and drain regions.

8. (Previously Presented) The method as set forth in claim 1, further comprising:

forming a trench in said semiconductor substrate; and

filling said trench with oxide to define an area in which a semiconductor device is to be fabricated.

9. (Withdrawn) A semiconductor device comprising:

(a) a semiconductor substrate;

(b) a first MOS transistor formed on said semiconductor substrate, and including semiconductor-metal compound formed in said semiconductor substrate;

(c) a second MOS transistor formed on said semiconductor substrate; and

(d) a film covering said second MOS transistor therewith for preventing semiconductor-metal compound from being formed in said semiconductor substrate.

10. (Withdrawn) The semiconductor device as set forth in claim 9, wherein said semiconductor substrate is a silicon substrate, and said semiconductor-metal compound is silicide.

11. (Withdrawn) The semiconductor device as set forth in claim 10, wherein metal in said semiconductor-metal compound is cobalt, tungsten or titanium.

12. (Withdrawn) The semiconductor device as set forth in claim 9, wherein said film is comprised of an oxide film.

13. (Withdrawn) The semiconductor device as set forth in claim 12, wherein said oxide film is formed by chemical vapor deposition (CVD) in the range of 300 to 500 degrees centigrade both inclusive by the thickness of 20 to 40 nanometers both inclusive.

14. (Withdrawn) The semiconductor device as set forth in claim 9, further comprising an interlayer insulating film including said film as a lower film, and wherein a wiring formed above said MOS transistor is electrically connected to said first MOS transistor through a contact plug formed throughout said interlayer insulating film, and said wiring is electrically connected to said second MOS transistor through a contact plug formed throughout said interlayer insulating film and said film.

15. (Previously Presented) The method as set forth in claim 1 wherein said semiconductor device includes a shallow trench isolation (STI) film.

16. (Previously Presented) A method of fabricating a semiconductor device, comprising, in sequence:

(a) forming a shallow trench isolation (STI) film on a semiconductor substrate;

(b) implanting impurity ions into a well region with a gate electrode and a sidewall both being used as a mask to form source/drain regions;

(c) forming an oxide film entirely over said semiconductor substrate on which a MOS transistor is fabricated;

(d) carrying out first thermal-annealing to said semiconductor substrate:

(e) selectively removing said oxide film in an area where later mentioned semiconductor-metal compound is to be formed while leaving said oxide film in a non-silicide transistor region;

(f) forming a metal film entirely over said semiconductor substrate; and

(g) carrying out second thermal-annealing to said semiconductor substrate to form semiconductor-metal compound in said area,

wherein no thermal-annealing steps are carried out between said (b) and (c) so as to prevent a recess at a shoulder of said shallow trench isolation film from deepening.

17. (Previously Presented) The method as set forth in claim 16, further comprising (f) removing said metal film having been not reacted with said semiconductor substrate.

18. (Previously Presented) The method as set forth in claim 16, wherein said semiconductor substrate is a silicon substrate, and said semiconductor-metal compound is silicide.

19. (Previously Presented) The method as set forth in claim 18, wherein said metal film is composed of cobalt, tungsten or titanium.

20. (Previously Presented) The method as set forth in claim 16, wherein said oxide film is formed by chemical vapor deposition (CVD) in the range of 300 to 500 degrees centigrade both inclusive by the thickness of 20 to 40 nanometers both inclusive.

21. (Previously Presented) The method as set forth in claim 16, wherein said first thermal-annealing is carried out as spike rapid thermal annealing (RTA) by zero second in the range of 1000 to 1100 degrees centigrade.

22. (Previously Presented) The method as set forth in claim 16, wherein said first thermal-annealing is carried out also for activating impurities having been implanted into source and drain regions of said MOS transistor, and for removing defects in said source and drain regions.